REMARKS/ARGUMENTS

Claims 1-15 are pending in this application.

Objection to the Declaration

The declaration is objected to as not identifying the filing of International Application PCT/US03/11627 on which priority is claimed. A supplemental Declaration in compliance with 37 CFR 1.63(c) including the identification of the filing of International Application PCT/US03/11627 was submitted on February 19, 2007. Therefore, this objection has been satisfied, and should be withdrawn.

Objection to the Drawings

Figure 1 has been objected to for omitting the legend "—Prior Art—." However, applicants respectfully submit that while Fig. 1 of the present claimed invention and Fig. 1 of Wang (U.S. Patent No. 6,266,380) may contain similar block diagram headings, the functions performed by the present claimed invention are different than the functions performed by Wang. More specifically, the present claimed invention in Fig. 1 contains block diagram #60 entitled "SEGMENT SYNC AND SYMBOL CLK. RECOVERY." This is similarly shown in Fig. 1 of Wang as block diagram #24. However, the two similarly titled blocks perform different methods of segmenting the synchronization and symbol clock recovery. In the present claimed invention, "the STR symbol frequency offset in the circuit 60 is set during the acquisition phase to different values chosen from the range of offsets that the STR is likely to traverse. In a preferred embodiment of the present invention the STR offset range is specified to be ± 1 kHz. This range is partioned into nine points which corresponds to offsets of 0, ± 200 Hz, ± 400 Hz, ± 600 Hz, and ± 800 Hz from the nominal symbol frequency" (Specification, page 8, lines 19-24). Block #24 in Fig. 1 of Wang "detects and separates the repetitive data segment sync components of each data frame from the random data" (Col. 2, lines 57-58). However, Wang does not specify the STR offset range to be partitioned into nine points, as in the present claimed invention. Therefore, the functions performed in Fig. 1 of the present claimed invention are different from the functions performed in Fig. 1 of Wang. Therefore, Fig. 1 of the present claimed invention is not illustrating a prior art system and applicants respectfully submit it would not be proper to identify the figure as such. In

view of the above remarks regarding Fig. 1 it is respectfully submitted that this objection is satisfied and should be withdrawn.

Rejection of Claims 1, 3-6, 8 and 10-14 under 35 USC § 102(b)

Claims 1, 3-6, 8 and 10-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Shanley (U.S. 4,617,587).

The present claimed invention provides a method and apparatus for establishing timing synchronism between a transmitter symbol clock and a local symbol clock in a receiver for receiving a signal transmitted as a sequence of symbols at a symbol frequency and subject to exhibiting a symbol frequency offset. A preselected number of offset values for a desired symbol timing recovery range are calculated. The offset values are grouped substantially symmetrically about a central offset value. Each of the preselected offset values is tested to see if symbol timing recovery lock can be achieved starting at the central offset value and gradually moving away from the central offset value. Independent claims 1 and 8 include features similar to those discussed above and thus the arguments presented below apply to each of these claims.

Shanley neither discloses nor suggests "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" as recited in the present claimed invention. Additionally, Shanley neither discloses nor suggests "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention.

Shanley's invention "relates generally to control loops for use in automatically establishing a desired condition of operation of electrical apparatus, and particularly to a recovery system for use with such a control loop to enable recovery from a failure mode in which a control voltage may be spuriously driven to a control voltage range extreme without establishing the desired operating condition" (Col. 1, lines 5-11).

Shanley describes "a control loop employed to effect color synchronization in a color television receiver" (Col. 1, lines 12-14). "The phase comparator and the phase shifted signal amplifier cooperate with the local color oscillator to form a phase locked loop, the loop functioning to lock the oscillator frequency and phase to the incoming color synchronizing bursts. When the free-running frequency of the oscillator is equal to the subcarrier frequency of the incoming synchronizing bursts ... accurate phasing of reference oscillations ... is readily attainable. However, when the phase locked loop achieves locking in instances where the free-running frequency of the local oscillator is not equal to the subcarrier frequency of the incoming bursts, the loop will have stabilized in a condition appropriate to achievement of an alteration of the oscillator frequency " (Col. 2, lines 18-37). When this occurs, a static phase error occurs (see Col. 2, lines 39-54) and the oscillator frequency is adjusted (see Col. 12, lines 16-24) for synchronization. Thus, Shanley merely synchronizes the free-running frequency of the local oscillator with the subcarrier frequency of the incoming bursts order to properly display colors in NTSC or PAL type television receivers (see Col. 2, lines 47-54). However, Shanley neither discloses nor suggests "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" as recited in the present claimed invention. Furthermore, as Shanley does not calculate offset values, Shanley also neither discloses nor suggests "testing each of the preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention.

The Office Action quotes Col. 12, lines 52-64 of Shanley as being equivalent to the present claimed invention. Applicants respectfully disagree. Shanley describes that "the recovery apparatus effectively functions to 'sweep' the oscillator's free-running frequency in discrete steps from a remote range edge frequency in a direction lessening the difference between the oscillator frequency and the subcarrier frequency. This sweep capability permits recovery from the consequences of a 'wrong-direction' start; the subsequent 'right-direction' sweep continues until the shifted pull-in range of the oscillator encompasses the subcarrier frequency, allowing lock to be attained by the phase locked loop (31, 32) during the burst comparisons of the succeeding field interval" (Col. 12, lines 53-64). Nowhere in the above cited passage or anywhere else in Shanley is there mention or suggestion of "calculating a

preselected number of offset values for a desired symbol timing recovery range" as recited in the present claimed invention. Furthermore, contrary to the assertions made in the Office Action, the "sweeps" performed in Shanley are not performed at a central offset value, as Shanley does not calculate any "offset values" and therefore, cannot group the offset values "substantially symmetrically about a central offset value" as in the present claimed invention. Additionally, as "a preselected number of offset values for a desired symbol timing recovery range" are not calculated by Shanley, Shanley also cannot test "each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention. Therefore, Shanley does not disclose or suggest the features of the present claimed invention.

In view of the above remarks regarding claims 1 and 8 it is respectfully submitted that Shanley does not anticipated the present invention as claimed in independent claims 1 and 8. As claims 3-6 and 10-14 are dependent on claims 1 and 8 respectively, it is respectfully submitted that these claims are also patentable for the same reasons as claims 1 and 8 discussed above. It is thus further respectfully submitted that this rejection is satisfied and should be withdrawn.

Rejection of Claims 2 and 9 Under 35 U.S.C 103(a)

Claims 2 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shanley (U.S. Patent No. 4,617,587) in view of Wang (U.S. Patent No. 6,266,380).

Wang, similar to Shanley, neither discloses nor suggests "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" as in the present claimed invention. Additionally, Wang, similar to Shanley, neither discloses nor suggests "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention.

Wang describes a system for eliminating DC offset in a received HDTV signal. A receiver processes a VSB modulated signal containing terrestrial broadcast high definition television information. A pilot component includes an input analog-to-digital converter for producing a datastream which is oversampled at twice the received symbol rate. A segment sync detector uses an abbreviated correlation reference pattern to recover a twice symbol rate sampling clock for the digital converter. A DC offset associated with the pilot component is removed from the demodulated signal before it is applied to an NTSC interference detection network. However, similar to Shanley, Wang neither discloses nor suggests "**calculating a preselected number of offset values for a desired symbol timing recovery range**, said offset values being grouped substantially symmetrically about a central offset value" as recited in the present claimed invention. Wang is concerned with attenuating DC component from a demodulated symbol datastream. This is unlike the present claimed invention which is concerned with establishing timing synchronism between a transmitter symbol clock and a local symbol clock in a receiver for receiving a signal transmitted as a sequence of symbols at a symbol frequency and subject to exhibiting a symbol frequency offset.

Additionally, since Wang is not concerned with calculating a preselected number of offset values for a desired symbol timing recover range, Wang also cannot disclose or suggest "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of present claimed invention. Wang describes a system for processing a received VSB signal containing high definition television information that includes a compensation network for processing an oversampled symbol datastream at the oversampling rate to remove a symbol DC offset component. Therefore, Wang is concerned with attenuating DC component from a demodulated symbol datastream. This is unlike the present claimed invention which provides a preselected number of offset values for testing to achieve a desired symbol timing recovery lock quickly and accurately. Thus, Wang neither discloses nor suggests "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of present claimed invention.

Applicants respectfully submit that there is no reason or motivation to combine Shanley with Wang. Shanley describes control loops for use in automatically establishing a desired condition of operation of electrical apparatus, and a recovery system for use with the control loop to enable recovery from a failure mode in which a control voltage may be spuriously driven to a control voltage range extreme without establishing the desired operating condition. Wang describes a system for eliminating DC offset from a demodulated symbol datastream. These references are responsive to different problems and thus, it is respectfully submitted that the combination of these references to produce the present invention would not be obvious. Shanley describes an "auxiliary apparatus" (Col. 4, line 1) that adjusts "the free-running frequency of the oscillator" (Col. 4, line 2) and keeps reducing "the difference relative to the burst subcarrier frequency" (Col. 4, lines 3-4) until "a convergence to a condition where the phase locked loop locks up with static phase error substantially completely eliminated" (Col. 4, lines 8-10). Wang, on the other hand, provides an improved method of "processing an oversampled symbol datastream at the oversampling rate to remove a symbol DC offset component" (Col. 1, lines 38-40). Shanley is not concerned with DC offset, as in Wang, and Wang is not concerned with converging to a condition where the free-running frequency of the oscillator is synchronized with the subcarrier frequency, as in Shanley.

However, even if these two references were combined, the combination of the system of Shanley with the system of Wang would not produce the present invention as claimed. Instead, the combined system would be an HDTV television receiver that synchronizes the free-running frequency of the oscillator with the subcarrier frequency to accurately avoid hue errors (or saturation errors) and eliminate DC offset in a VSB modulated signal. This is wholly unlike the present claimed invention. Specifically, the present claimed invention recites "**calculating a preselected number of offset values for a desired symbol timing recovery range**, said offset values being grouped substantially symmetrically about a central offset value." The combined system of Shanley and Wang, similarly to the individual systems, neither discloses nor suggests such features. Consequently, it is respectfully submitted that the present invention as claimed is patentable over the cited reference when taken alone or in combination.

In view of the above remarks, it is respectfully submitted that there is no 35 USC 112 enabling disclosure in Shanley or Wang, when taken alone or in combination, which would make claims 2 and 9 of the present claimed invention unpatentable. Thus, it is further respectfully submitted that this rejection is satisfied and should be withdrawn.

Rejection of Claims 7 and 15 Under 35 U.S.C 103(a)

Claims 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shanley (U.S. Patent No. 4,617,587) in view of Guillemain et al (U.S. Patent No. 6,175,600).

Guillemain, similar to Shanley, neither discloses nor suggests "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" as in the present claimed invention. Additionally, Guillemain, similar to Shanley, neither discloses nor suggests "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention.

Guillemain describes a system for detecting the presence of a carrier wave in a digital signal that is available at a given frequency. The system delivers at least two baseband samples of the digital signal at each symbol time. A timing estimator responds to the baseband samples to provide an error signal corresponding to a phase error between the clock frequency that is to be recovered and a local clock frequency. A detection signal is generated when a level representative of the variance of the error signal reaches a threshold value. However, similar to Shanley, Guillemain neither discloses nor suggests "**calculating a preselected number of offset values for a desired symbol timing recovery range**, said offset values being grouped substantially symmetrically about a central offset value" as recited in the present claimed invention. Guillemain is concerned with detecting the presence or the absence of a signal carrier wave that is present at a given clock frequency. This is unlike the present claimed invention which is concerned with establishing timing synchronism between a transmitter symbol clock and a local symbol clock in a receiver for receiving a signal transmitted as a sequence of symbols at a symbol frequency and subject to exhibiting a symbol frequency offset.

Additionally, since Guillemain is not concerned with calculating a preselected number of offset values for a desired symbol timing recover range, Guillemain also cannot disclose or suggest "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of present claimed invention. Guillemain describes a timing estimator responsive to the baseband samples for delivering an error signal corresponding to the phase error between the clock frequency that is to be recovered and a local frequency. A detector generates a detection signal indicating that a carrier wave has been detected whenever a level representative of the variance of the error signal reaches a threshold value. Therefore, Guillemain is concerned with detecting the presence of a carrier wave in a digital signal that is available at a given frequency. This is wholly unlike the present claimed invention which provides a preselected number of offset values for testing to achieve a desired symbol timing recovery lock quickly and accurately. Thus, Guillemain neither discloses nor suggests "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of present claimed invention.

Applicants respectfully submit that there is no reason or motivation to combine Shanley with Guillemain. Shanley describes control loops for use in automatically establishing a desired condition of operation of electrical apparatus, and a recovery system for use with the control loop to enable recovery from a failure mode in which a control voltage may be spuriously driven to a control voltage range extreme without establishing the desired operating condition. Guillemain describes a system detecting the presence of a carrier wave in a digital signal that is available at a given frequency. These references are responsive to different problems and thus, it is respectfully submitted that the combination of these references to produce the present invention would not be obvious. Shanley describes an "auxiliary apparatus" (Col. 4, line 1) that adjusts "the free-running frequency of the oscillator" (Col. 4, line 2) and keeps reducing "the difference relative to the burst subcarrier frequency" (Col. 4, lines 3-4) until "a convergence to a condition where the phase locked loop locks up with static phase error substantially completely eliminated" (Col. 4, lines 8-10).

Guillemain, on the other hand, provides an improved method of detecting the presence of a signal carrier wave that combines "speed, reliability, operation at a poor ED/No ratio (close to 2 dB), and is relatively insensitive to drift in the frequency of the carrier wave" (col. 2, lines 23-29).

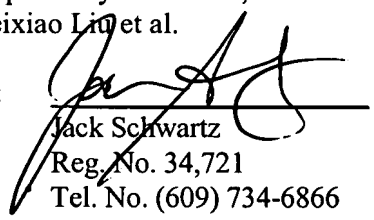
However, even if the systems of Shanley and Guillemain were combined, the combined system would not produce the present invention as claimed. Instead, the combined system would yield a system that synchronizes the free-running frequency of the oscillator with the subcarrier frequency to accurately avoid hue errors (or saturation errors) in a television system and detects the presence or absence of a signal carrier wave at a given frequency. This is wholly unlike the present claimed invention. Specifically, the present claimed invention recites "**calculating a preselected number of offset values for a desired symbol timing recovery range**, said offset values being grouped substantially symmetrically about a central offset value." The combined system of Shanley and Guillemain, similarly to the individual systems, neither discloses nor suggests such features. Consequently, it is respectfully submitted that the present invention as claimed is patentable over the cited reference when taken alone or in combination.

In view of the above remarks, it is respectfully submitted that there is no 35 USC 112 enabling disclosure in Shanley and Guillemain, when taken alone or in combination, which would make claims 7 and 15 of the present claimed invention unpatentable. Thus, it is further respectfully submitted that this rejection is satisfied and should be withdrawn.

Having fully addressed the Examiner's rejections, it is believed that, in view of the preceding remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at the phone number below, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed due. However, if a fee is due, please charge the additional fee to Deposit Account 07-0832.

Respectfully submitted,
Weixiao Liu et al.

By: 
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